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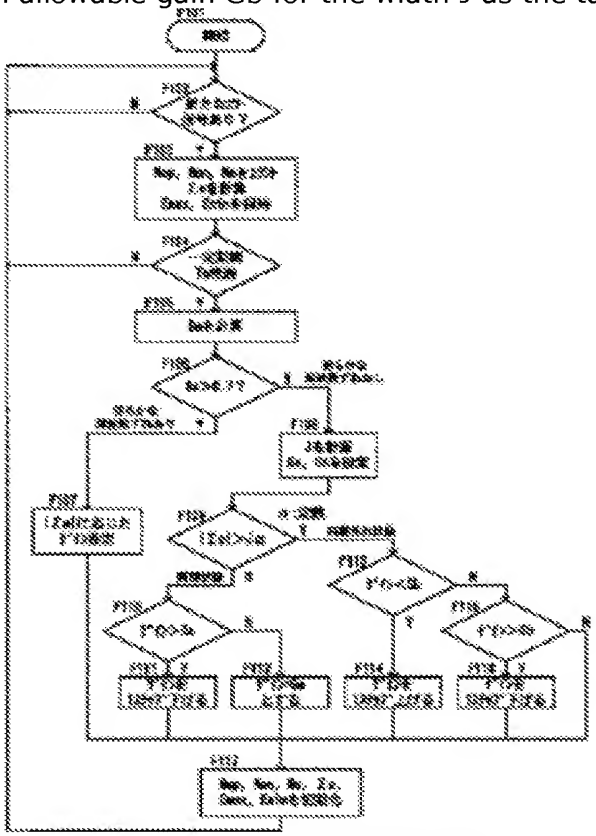
Abstract:
PROBLEM TO BE SOLVED: To perform quick pull into synchronism, when clear frequency deviation exists between the frequency of a reproduction clock and frequency of a data reproduction side by performing gain setting, on the basis of the distribution state of a plurality of error signals.SOLUTION: Whether an input signal synchronizes with a reproduction clock is discriminated on the basis of the relation between the absolute value of the total amount Sigmae of error signals outputted in a prescribed period Ta and a jitter width J (F109). Here, when the input signal and the production clock are in synchronous state, gain is changed with a stable gain Ga for the width J as a target value, and when they are not in synchronous state, the gain is changed with an allowable gain Gb for the width J as the target value.



JPO Machine translation abstract:
(57) **Abstract**
SUBJECT A reproduction clock becomes unstable when the jitter has occurred in the input signal in the clock reproduction circuit which obtains the reproduction clock which synchronized the coding equipment side based on the time reference information transmitted with data.
Means for Solution Based on a relation of an absolute value of total sigmae of an error signal and jitter width J which were outputted to prescribed period Ta, It distinguishes whether an input signal and a reproduction clock are in a synchronous state (F109), in being in a synchronous state, it changes a gain by making the stable gain Ga over jitter width J into a desired value, and when there is nothing to a synchronous state, a gain is changed by making the permissible gain Gb over jitter width J into a desired value.

Claim(s)
Claim 1 Have the following and it is distinguished whether said gain setting means has a frequency drift clear between frequency of said reproduction clock, and frequency by the side of generation of said data based on a distributed situation of two or more of said error signals, A clock reproduction circuit changing a gain value in said variable gain means according to this discriminated result.
An error signal creating means which is a clock reproduction circuit which generates a reproduction clock which

synchronized the generation side of said data based on time reference information transmitted with data, and generates an error signal based on said reproduction clock and said time reference information in input data.
A variable gain means which can give a gain of variable quantity to said error signal.
A gain setting means which sets up a gain value in said variable gain means based on two or more error signals from said error signal creating means.
A clock generating means which generates said reproduction clock based on an error signal which said variable gain means outputs.

Claim 2 When there was no frequency drift clear between frequency of said reproduction clock and frequency by the side of generation of said data and it is distinguished, said gain setting means, The clock reproduction circuit according to claim 1 changing a gain value in said variable gain means according to jitter width in said two or more error signals.
Claim 3 When there was no frequency drift clear between frequency of said reproduction clock and frequency by the side of generation of said data and it is distinguished, said gain setting means, It is judged whether in a relation of total and said jitter width of said error signal in a prescribed period, the generation side of said reproduction clock and said data is in a synchronous state, When it is in a synchronous state, while changing a gain value towards the 1st desired value set up based on said jitter width, The clock reproduction circuit according to claim 2 changing a gain value towards the 2nd desired value as for which is set up based on said jitter width when there is nothing to a synchronous state, and size becomes from said 1st desired value.
Claim 4 When there was a frequency drift clear between frequency of said reproduction clock and frequency by the side of generation of said data based on a distributed situation of two or more of said error signals and it is distinguished, said gain setting means, The clock reproduction circuit according to claim 1 changing a gain value in said variable gain means according to total of said error signal in a prescribed period.
Claim 5 When there was no frequency drift clear between frequency of said reproduction clock and frequency by the side of generation of said data based on a distributed situation of two or more of said error signals and it is distinguished, said gain setting means, The clock reproduction circuit according to claim 1 lowering a gain value in said variable gain means.

Detailed Description of the Invention
0001
Field of the Invention The MPEG2 transport stream which carries data storage or digital broadcasting receivers, such as D-VHS (registered trademark) in which a bus connection is possible. It is a clock reproduction circuit in the decoder of (describing it as "MPEG 2-TS" hereafter), etc., and is related with the suitable clock reproduction circuit for the apparatus which receives MPEG 2-TS having contained the jitter.
0002
Description of the Prior Art At the stream of MPEG 2-TS, the time reference information called PCR (Program Clock Reference) is inserted in about 0.1 second by 1 times or more of frequency. Although generation addition is carried out with the coding equipment of MPEG 2-TS, this PCR, In the decoding machine which decodes MPEG 2-TS, in order to reproduce a video signal and an audio signal correctly, with reference to this PCR, it is necessary to generate the system clock of coding equipment, and the system clock which synchronized.
0003 An example of such a clock reproduction circuit of MPEG 2-TS is shown in drawing 4. The subtraction machine with which 1 outputs an error signal in the figure based on the PCR value extracted from MPEG 2-TS, and the STC (System Time Clock) value outputted from the STC counter 2, The gain circuit which 3 gives a predetermined gain to the error signal from the subtraction machine 1, and is outputted, and 4 are digital LPF which performs filtering to the output of the gain circuit 3, and outputs this.
0004 The D/A converter which 5 changes the output of digital LPF4 into an analog signal, and is outputted, and 6 are voltage controlled oscillators (VCXO) which output the clock of frequency which changes according to the voltage of the analog signal outputted from D/A converter 5 by making 27 MHz into center frequency. And the STC value which the output of the voltage controlled oscillator 6 is outputted to the decoding machine of MPEG 2-TS as a system clock, and it is outputted to the STC counter 2, and the STC counter 2 outputs is supplied to the subtraction machine 1.
0005 The subtraction machine 1 sets PCR (n) and the STC value at the time to STC (n) for the PCR value received at a certain time, When PCR (n-1) and the STC value at that time are set to STC (n-1) for the PCR value received just before that, the value which subtracted PCR (n) to PCR (n-1) is compared with the value which subtracted STC (n) to STC (n-1), and the difference value of these two values is outputted.
0006 Here, the PCR value inserted in MPEG 2-TS is a value which counted a 27-MHz frequency clock and was given in coding equipment.
Since the STC value which the STC counter 2 outputs is also a value outputted from the voltage controlled oscillator 6 which made 27 MHz center frequency, If the clock frequency by the side of coding equipment and the clock frequency from the voltage controlled oscillator 6 are thoroughly in agreement, the error signal of the subtraction machines 1-0 will be outputted, but when a frequency drift is among both clocks, the error signal according to this gap will be outputted.

0007 The feedback loop is formed with the above composition, and it is controlled so that the same clock as the

clock by the side of coding equipment is outputted from the voltage controlled oscillator 6.

0008

Problem to be solved by the invention However, when MPEG 2-TS is received via a bus, the packet interval of MPEG 2-TS may be changed by a difference and transmission format of a transmission clock. For this reason, in reception through a transmission line like a bus, packet reception will be performed in the state where it was superimposed on the jitter.

0009 If TS having contained the big jitter is received when the conventional clock reproduction circuit is used and the gain in the gain circuit 3 is set up highly here, the frequency of the system clock which the voltage controlled oscillator 6 outputs will be changed sharply, and it will become unstable operating it.

0010 When TS containing a jitter was assumed, the gain was set up low, but quick synchronous drawing in was not able to be performed in this case. Even if it was after synchronous drawing in, the synchronous gap called what is called a drift may occur, and, in such a case, quick synchronous drawing in was not able to be performed. Thus, when MPEG 2-TS was overlapped on the jitter, it was difficult to make the gain set value of the gain circuit 3 into a suitable value.

0011

Means for solving problem In order to solve the above SUBJECT, the clock reproduction circuit concerning this invention, It is a clock reproduction circuit which generates the reproduction clock which synchronized the generation side of said data based on the time reference information transmitted with data, The error signal creating means which generates an error signal based on said reproduction clock and said time reference information in input data, The variable gain means which can give the gain of variable quantity to said error signal, The gain setting means which sets up the gain value in said variable gain means based on two or more error signals from said error signal creating means, Have a clock generating means which generates said reproduction clock based on the error signal which said variable gain means outputs, and said gain setting means, It distinguishes whether based on the distributed situation of two or more of said error signals, there is any frequency drift clear between the frequency of said reproduction clock and the frequency by the side of generation of said data, and the gain value in said variable gain means is changed according to this discriminated result.

0012 When there was no frequency drift with a clock reproduction circuit clear between the frequency of said reproduction clock and the frequency by the side of generation of said data concerning this invention and it is distinguished, said gain setting means, According to the jitter width in said two or more error signals, the gain value in said variable gain means is changed.

0013 When there was no frequency drift with a clock reproduction circuit clear between the frequency of said reproduction clock and the frequency by the side of generation of said data concerning this invention and it is distinguished, said gain setting means, It is judged whether in the relation of total and said jitter width of said error signal in a prescribed period, the generation side of said reproduction clock and said data is in a synchronous state, When it is in a synchronous state, while changing a gain value towards the 1st desired value set up based on said jitter width, when there is nothing to a synchronous state, it is set up based on said jitter width, and size is characterized by changing a gain value towards the 2nd becoming desired value from said 1st desired value.

0014 When the clock reproduction circuit concerning this invention had a frequency drift clear between the frequency of said reproduction clock, and the frequency by the side of generation of said data based on the distributed situation of two or more of said error signals and it is distinguished, Said gain setting means changes the gain value in said variable gain means according to total of said error signal in a prescribed period.

0015 When the clock reproduction circuit concerning this invention did not have the frequency drift clear between the frequency of said reproduction clock, and the frequency by the side of generation of said data based on the distributed situation of two or more of said error signals and it is distinguished, Said gain setting means lowers the gain value in said variable gain means.

0016

Mode for carrying out the invention Even if it is a clock reproduction circuit concerning this invention at the input time of MPEG 2-TS having contained the comparatively big jitter, it synchronizes a system clock with the system clock by the side of coding equipment for a short time, and. The system clock stable where synchronous drawing in is completed was obtained.

0017 The composition of the clock reproduction circuit concerning this invention adds the composition of the gain setting circuit 7 to the clock reproduction circuit shown by drawing 4, as shown in drawing 1. That is, about the composition and operation of subtraction machine 1, STC counter 2, gain circuit 3, and digital LPF4, D/A converter 5, and the voltage controlled oscillator 6, since it already explained, the explanation is omitted, and operation of the gain setting circuit 7 is mainly explained here.

0018 As shown in drawing 1, the error signal from the subtraction machine 1 is inputted into the gain setting circuit 7, and based on this error signal, the gain setting circuit 7 is constituted so that the gain in the gain circuit 3 may be set up.

0019 Drawing 2 is a flow chart for explaining the setting-operation of the gain in the gain circuit 3 set up by the gain setting circuit 7. When MPEG 2-TS was inputted (F101), it is detected whether a new error signal was inputted first (F102) and a new error signal is detected in the figure, While progressing to Y, when not being detected, the detecting operation is repeated until a new error signal is detected.

0020 Next, when a new error signal is detected. The positive error number Nep in an error signal, negative error number Nen, total-number-of-error Ne, and error total sigmae are calculated, and the maximum Emax of

an error and the minimum Emin of an error are held (F103), and it is detected whether fixed time Ta was reached after that (F104).

0021 And when fixed time Ta is reached, while progressing to Y, when fixed time Ta is not reached, it progresses to N. That is, when fixed time Ta is not reached, operation of F102 and F103 is repeated until it reaches fixed time Ta.

0022 Since PCR in MPEG 2-TS is inserted in at least 0.1 second by 1 time of frequency if fixed time Ta in F104 is set up for 1 second here, after about ten error signals are detected in fixed time Ta in this case, it will progress to processing of F105.

0023 Although the error number Nep positive whenever a new error signal is detected, negative error number Nen, total-number-of-error Ne, and error total sigmae are calculated and the maximum Emax of an error and the minimum Emin of an error are held in F103, Processing after F105 is performed after fixed time Ta has passed.

0024 Drawing 3 is a figure showing the error signal detected in fixed time Ta, and shows the case where the figure (a) has a large frequency drift between a system clock and the system clock by the side of coding equipment, and the figure (b) shows the case where a frequency drift is small. The figure (c) shows the state where the big jitter is included, although a frequency drift is small.

0025in addition -- as opposed to ten error signals in fixed time Ta in an example shown in the figure (a) -- the positive error number Nep -- 9 and the negative error number Nen are set to one, and, as for the maximum Emax of 44 and an error, as for the total number of error Ne, in 10 and error total sigmae, the minimum Emin of 9 and an error has become -1. And based on these values, the bias Be of error distribution is calculated as follows (F105).

Be=|(Nep-Nen)|/Ne**0026**Here, when the bias Be of error distribution is close to a value of one, it can be judged that a gap has arisen in frequency of a system clock and a system clock by the side of coding equipment clearly. That is, when error distribution in fixed time Ta inclines for Masakata or toward either one of a negative direction greatly, it can be judged that a frequency drift has arisen clearly.

0027 In a clock reproduction circuit concerning this invention, it judged that a clear frequency drift would have occurred, for example on the basis of 0.7 if a value of the bias Be of error distribution is a larger value than 0.7 (F106), and if it is 0.7 or less value, it will be judged that a clear frequency drift is not generated. That is, in an example shown in drawing 3 (a), a value of the bias Be of error distribution is 0.8, and is judged that a clear frequency drift has arisen.

0028 And when it is judged that the clear frequency drift has occurred, the gain in the gain circuit 3 is set as the value according to the absolute value of error total sigmae (F107). That is, according to the size of the absolute value of error total sigmae, selection setting of the one step in the gain which can be set as two or more steps is carried out. In the example shown in drawing 3 (a), since the value of error total sigmae is 44, it is set as the gain of the step according to this value.

0029 On the other hand, when the value of the bias Be of error distribution is 0.7 or less value in F106, jitter width J is calculated after that, and the stable gain Ga over jitter width J and the permissible gain Gb over jitter width J are set up (F108). That is, as shown in drawing 3 (b), in the case of error distribution, since the value of the bias Be of error distribution is 0.2, it is judged that the clear frequency drift is not produced, but a big jitter may be included even when the frequency drift has not arisen. Therefore, it is necessary to set up the gain according to jitter width.

0030 Here, when the gain which can obtain a stable clock to certain jitter width J is searched for experimentally, if jitter width doubles, it turns out that a stable gain serves as half. That is, since the stable gain Ga over jitter width J is in inverse proportion to jitter width J, it becomes as follows.

Ga=a/J (a is a constant)

0031 Since it turns out that it is similarly in inverse proportion to jitter width J when the permissible gain to which a clock is not sharply changed too much to certain jitter width J is searched for experimentally, it becomes as follows.

Gb=b/J (b is a constant)

0032 Although the stable gain Ga and the permissible gain Gb can be set up by defining the above constants a and b by an experiment or an operation beforehand, Since the stable gain Ga is a permissible gain to which, as for the permissible gain Gb, a clock is not sharply changed too much to being a gain which can obtain a stable clock, the relation between the stable gain Ga and the permissible gain Gb becomes as follows.

The thing which is Ga<Gb and for which these values are beforehand held in equipment is also possible.

0033 Next, a step-out is detected by comparing the threshold proportional to jitter width J with the absolute value of error total sigmae. That is, when the absolute value of error total sigmae is over value Jalpha which multiplied jitter width J by the predetermined constant alpha like the graphic display, while judging that it is in a step-out state, in being below value Jalpha which multiplied jitter width J by the predetermined constant alpha, it judges that it is in the state which was able to take the synchronization (F109).

0034 Thus, in the clock reproduction circuit concerning this invention, when jitter width J is a large value, even if the absolute value of error total sigmae is comparatively large, it is judged that it is in the state which was able to take the synchronization. This is for preventing judging it as a step-out under the influence of this big jitter, even if it is in the tendency for the absolute value of error total sigmae to turn into a big value by this big jitter and is a synchronous state, when a big jitter occurs suddenly.

0035 Here, although drawing 3 (c) has taken the synchronization, it shows the state where the big jitter occurred suddenly. Thus, when a big jitter occurs suddenly, the absolute value of error total sigmae turns into a

big value under the influence of this jitter, but he judges this state to be a synchronous state, and is trying to avoid unnecessary gain fluctuation in the clock reproduction circuit concerning this invention.

0036 In order to cope with such a big jitter that carries out the heterogenesis, It may be made to judge using the value of two or more error total not only in error total sigmae in fixed time Ta but this or before by calculating error total over a period longer than fixed time Ta whether it is a synchronous state.

0037 Next, when it is judged that it is in the state which was able to take the synchronization. When the present gain set value is compared with the stable gain Ga over jitter width J (F110) and the present gain set value is over the stable gain Ga, When 1 step lowering (F111) and the present gain set value are below the stable gain Ga about the present gain set value, the present gain is set as the stable gain Ga. Thus, in the state where the synchronization can be taken, a gain is changed in the direction which brings the present gain set value close to the stable gain Ga over jitter width J.

0038 It is 1 step ****** (F114) about the gain set value of the present when the present gain set value is compared with the permissible gain Gb over jitter width J on the other hand when it is distinguished that it is in a step-out state (F113), and the present gain set value is less than the permissible gain Gb.

0039 When the present gain set value is beyond the permissible gain Gb, When the present gain set value is over the permissible gain Gb as compared with the permissible gain Gb (F115), the present gain set value, A gain is not changed when 1 step lowering (F116) and the present gain set value are below the permissible gain Gb about the present gain set value (i.e., when the present gain set value is the same as that of the permissible gain Gb). That is, in a step-out state, a gain is changed in the direction which brings the present gain set value close to the permissible gain Gb over jitter width J.

0040 After performing the above gain control, the maximum Emax of the positive error number Nep, negative error number Nen, total-number-of-error Ne, error total sigmae, and an error and the minimum Emin of an error are initialized (F117), and detection of the new error signal in F102 is resumed.

0041 Thus, in the clock reproduction circuit concerning this invention. Since it judges whether it is a synchronous state in the relation between jitter width J and the absolute value of error total and a gain is changed into the suitable desired value according to jitter width J in each state, Even when the big jitter has occurred in input MPEG 2-TS, the gain in the gain circuit 3 can be set as a suitable value.

0042 And after the value of an error signal is adjusted with the gain set up by doing in this way, it becomes possible to supply the analog signal through digital LPF4 and D/A converter 5 to the voltage controlled oscillator 6, and to obtain quickly the clock which synchronized with the system clock by the side of coding equipment.

0043 When the clear frequency drift had not occurred in F106 in drawing 2 in the above embodiment and it is distinguished, Although the example which performed gain setting according to jitter width was shown, when not only this but the clear frequency drift had not occurred and it is distinguished (i.e., when it is a with a value of 0.7 or less of the bias Be of error distribution value in F106), method control of 1 step ****** may be simply performed for a gain. It becomes possible it to become possible to make a suitable gain set up to the jitter of the grade which is also such control, and to make data processing reduce.

0044 It cannot be overemphasized that it does not matter whether the composition for performing the above gain setting processing is the composition by hardware or is the composition by software. It cannot be overemphasized that the clock reproduction circuit concerning this invention is applicable to image audio equipment, such as D-VHS (registered trademark) provided with the bus interface based on IEEE1394 and a set top box, or other connection devices.

0045

Effect of the Invention According to the clock reproduction circuit by this invention, since gain setting is performed based on the distributed situation of two or more error signals, when there is a frequency drift clear between the frequency of a reproduction clock and the frequency by the side of data reproduction, it becomes possible to perform quick synchronous drawing in.

0046 Since gain setting according to the jitter width in two or more error signals is performed, Even when the big jitter has occurred in input data, gain setting according to this jitter can be performed, and the effect that a good reproduction clock can be obtained also in the state where the jitter is generated is done so.

0047 Since it judges whether input data and a reproduction clock are in a synchronous state in the relation of the total and jitter width of an error signal in a prescribed period period according to the clock reproduction circuit by this invention, Even when a big jitter occurs suddenly, it can be judged correctly whether it is a synchronous state.

0048 When it is in a synchronous state, while changing a gain value towards the 1st desired value set up based on jitter width, Since a gain value is changed towards the 2nd desired value that is set up based on jitter width and as for which size becomes from the 1st desired value when there is nothing to a synchronous state, quick synchronous drawing in and generation of the stable reproduction clock after synchronous drawing in are attained.

0049 When there was no frequency drift clear between the frequency of a reproduction clock and the frequency by the side of data reproduction based on the distributed situation of two or more error signals and it is distinguished, suitable gain setting becomes possible by performing processing which lowers a gain, without performing much data processing.

Field of the Invention The MPEG2 transport stream which carries data storage or digital broadcasting

receivers, such as D-VHS (registered trademark) in which a bus connection is possible. It is a clock reproduction circuit in the decoder of (describing it as "MPEG 2-TS" hereafter), etc., and is related with the suitable clock reproduction circuit for the apparatus which receives MPEG 2-TS having contained the jitter.
0002

Description of the Prior Art At the stream of MPEG 2-TS, the time reference information called PCR (Program Clock Reference) is inserted in about 0.1 second by 1 times or more of frequency. Although generation addition is carried out with the coding equipment of MPEG 2-TS, this PCR, In the decoding machine which decodes MPEG 2-TS, in order to reproduce a video signal and an audio signal correctly, with reference to this PCR, it is necessary to generate the system clock of coding equipment, and the system clock which synchronized.
0003 An example of such a clock reproduction circuit of MPEG 2-TS is shown in drawing 4. The subtraction machine with which 1 outputs an error signal in the figure based on the PCR value extracted from MPEG 2-TS, and the STC (System Time Clock) value outputted from the STC counter 2, The gain circuit which 3 gives a predetermined gain to the error signal from the subtraction machine 1, and is outputted, and 4 are digital LPF which performs filtering to the output of the gain circuit 3, and outputs this.
0004 The D/A converter which 5 changes the output of digital LPF4 into an analog signal, and is outputted, and 6 are voltage controlled oscillators (VCXO) which output the clock of frequency which changes according to the voltage of the analog signal outputted from D/A converter 5 by making 27 MHz into center frequency. And the STC value which the output of the voltage controlled oscillator 6 is outputted to the decoding machine of MPEG 2-TS as a system clock, and it is outputted to the STC counter 2, and the STC counter 2 outputs is supplied to the subtraction machine 1.
0005 The subtraction machine 1 sets PCR (n) and the STC value at the time to STC (n) for the PCR value received at a certain time, When PCR (n-1) and the STC value at that time are set to STC (n-1) for the PCR value received just before that, the value which subtracted PCR (n) to PCR (n-1) is compared with the value which subtracted STC (n) to STC (n-1), and the difference value of these two values is outputted.
0006 Here the PCR value inserted in MPEG 2-TS, Since it is the value which counted a 27-MHz frequency clock and was given in coding equipment and the STC value which the STC counter 2 outputs is also a value outputted from the voltage controlled oscillator 6 which made 27 MHz center frequency, If the clock frequency by the side of coding equipment and the clock frequency from the voltage controlled oscillator 6 are thoroughly in agreement, the error signal of the subtraction machines 1-0 will be outputted, but when a frequency drift is among both clocks, the error signal according to this gap will be outputted.
0007 The feedback loop is formed with the above composition, and it is controlled so that the same clock as the clock by the side of coding equipment is outputted from the voltage controlled oscillator 6.
0008

Effect of the Invention According to the clock reproduction circuit by this invention, since gain setting is performed based on the distributed situation of two or more error signals, when there is a frequency drift clear between the frequency of a reproduction clock and the frequency by the side of data reproduction, it becomes possible to perform quick synchronous drawing in.
0046 Since gain setting according to the jitter width in two or more error signals is performed, Even when the big jitter has occurred in input data, gain setting according to this jitter can be performed, and the effect that a good reproduction clock can be obtained also in the state where the jitter is generated is done so.
0047 Since it judges whether input data and a reproduction clock are in a synchronous state in the relation of the total and jitter width of an error signal in a prescribed period period according to the clock reproduction circuit by this invention, Even when a big jitter occurs suddenly, it can be judged correctly whether it is a synchronous state.
0048 When it is in a synchronous state, while changing a gain value towards the 1st desired value set up based on jitter width, Since a gain value is changed towards the 2nd desired value that is set up based on jitter width and as for which size becomes from the 1st desired value when there is nothing to a synchronous state, quick synchronous drawing in and generation of the stable reproduction clock after synchronous drawing in are attained.
0049 When there was no frequency drift clear between the frequency of a reproduction clock and the frequency by the side of data reproduction based on the distributed situation of two or more error signals and it is distinguished, suitable gain setting becomes possible by performing processing which lowers a gain, without performing much data processing.

Problem to be solved by the invention However, when MPEG 2-TS is received via a bus, the packet interval of MPEG 2-TS may be changed by a difference and transmission format of a transmission clock. For this reason, in reception through a transmission line like a bus, packet reception will be performed in the state where it was superimposed on the jitter.

0009 If TS having contained the big jitter is received when the conventional clock reproduction circuit is used and the gain in the gain circuit 3 is set up highly here, the frequency of the system clock which the voltage controlled oscillator 6 outputs will be changed sharply, and it will become unstable operating it.
0010 When TS containing a jitter was assumed, the gain was set up low, but quick synchronous drawing in was not able to be performed in this case. Even if it was after synchronous drawing in, the synchronous gap called what is called a drift may occur, and, in such a case, quick synchronous drawing in was not able to be performed. Thus, when MPEG 2-TS was overlapped on the jitter, it was difficult to make the gain set value of the gain circuit 3 into a suitable value.
0011

Means for solving problem In order to solve the above SUBJECT, the clock reproduction circuit concerning this invention, It is a clock reproduction circuit which generates the reproduction clock which synchronized the generation side of said data based on the time reference information transmitted with data, The error signal creating means which generates an error signal based on said reproduction clock and said time reference information in input data, The variable gain means which can give the gain of variable quantity to said error signal, The gain setting means which sets up the gain value in said variable gain means based on two or more error signals from said error signal creating means, Have a clock generating means which generates said reproduction clock based on the error signal which said variable gain means outputs, and said gain setting means, It distinguishes whether based on the distributed situation of two or more of said error signals, there is any frequency drift clear between the frequency of said reproduction clock and the frequency by the side of generation of said data, and the gain value in said variable gain means is changed according to this discriminated result.
0012 When there was no frequency drift with a clock reproduction circuit clear between frequency of said reproduction clock and frequency by the side of generation of said data concerning this invention and it is distinguished, said gain setting means, According to jitter width in said two or more error signals, a gain value in said variable gain means is changed.
0013 When there was no frequency drift with a clock reproduction circuit clear between frequency of said reproduction clock and frequency by the side of generation of said data concerning this invention and it is distinguished, said gain setting means, It is judged whether in a relation of total and said jitter width of said error signal in a prescribed period, the generation side of said reproduction clock and said data is in a synchronous state, When it is in a synchronous state, while changing a gain value towards the 1st desired value set up based on said jitter width, when there is nothing to a synchronous state, it is set up based on said jitter width, and size is characterized by changing a gain value towards the 2nd becoming desired value from said 1st desired value.
0014 When a clock reproduction circuit concerning this invention had a frequency drift clear between frequency of said reproduction clock, and frequency by the side of generation of said data based on a distributed situation of two or more of said error signals and it is distinguished, Said gain setting means changes a gain value in said variable gain means according to total of said error signal in a prescribed period.
0015 When the clock reproduction circuit concerning this invention did not have the frequency drift clear between the frequency of said reproduction clock, and the frequency by the side of generation of said data based on the distributed situation of two or more of said error signals and it is distinguished, Said gain setting means lowers the gain value in said variable gain means.
0016
Mode for carrying out the invention Even if it is a clock reproduction circuit concerning this invention at the input time of MPEG 2-TS having contained the comparatively big jitter, it synchronizes a system clock with the system clock by the side of coding equipment for a short time, and. The system clock stable where synchronous drawing in is completed was obtained.
0017 The composition of the clock reproduction circuit concerning this invention adds the composition of the gain setting circuit 7 to the clock reproduction circuit shown by drawing 4, as shown in drawing 1. That is, about the composition and operation of subtraction machine 1, STC counter 2, gain circuit 3, and digital LPF4, D/A converter 5, and the voltage controlled oscillator 6, since it already explained, the explanation is omitted, and operation of the gain setting circuit 7 is mainly explained here.
0018 As shown in drawing 1, the error signal from the subtraction machine 1 is inputted into the gain setting circuit 7, and based on this error signal, the gain setting circuit 7 is constituted so that the gain in the gain circuit 3 may be set up.
0019 Drawing 2 is a flow chart for explaining the setting-operation of the gain in the gain circuit 3 set up by the gain setting circuit 7. When MPEG 2-TS was inputted (F101), it is detected whether a new error signal was inputted first (F102) and a new error signal is detected in the figure, While progressing to Y, when not being detected, the detecting operation is repeated until a new error signal is detected.
0020 Next, when a new error signal is detected. The positive error number Nep in an error signal, negative error number Nen, total-number-of-error Ne, and error total sigmae are calculated, and the maximum Emax of an error and the minimum Emin of an error are held (F103), and it is detected whether fixed time Ta was reached after that (F104).
0021 And when fixed time Ta is reached, while progressing to Y, when fixed time Ta is not reached, it

progresses to N. That is, when fixed time Ta is not reached, operation of F102 and F103 is repeated until it reaches fixed time Ta.

0022 Since PCR in MPEG 2-TS is inserted in at least 0.1 second by 1 time of frequency if fixed time Ta in F104 is set up for 1 second here, after about ten error signals are detected in fixed time Ta in this case, it will progress to processing of F105.

0023 Although the error number Nep positive whenever a new error signal is detected, negative error number Nen, total-number-of-error Ne, and error total sigmae are calculated and the maximum Emax of an error and the minimum Emin of an error are held in F103, Processing after F105 is performed after fixed time Ta has passed.

0024 Drawing 3 is a figure showing the error signal detected in fixed time Ta, and shows the case where the figure (a) has a large frequency drift between a system clock and the system clock by the side of coding equipment, and the figure (b) shows the case where a frequency drift is small. The figure (c) shows the state where the big jitter is included, although a frequency drift is small.

0025in addition -- as opposed to ten error signals in fixed time Ta in the example shown in the figure (a) -- the positive error number Nep -- 9 and the negative error number Nen are set to one, and, as for the maximum Emax of 44 and an error, as for the total number of error Ne, in 10 and error total sigmae, the minimum Emin of 9 and an error has become -1. And based on these values, the bias Be of error distribution is calculated as follows (F105).

Be=|(Nep-Nen)|/Ne**0026**Here, when the bias Be of error distribution is close to the value of one, it can be judged that the gap has arisen in the frequency of a system clock and the system clock by the side of coding equipment clearly. That is, when the error distribution in fixed time Ta inclines for Masakata or toward either one of a negative direction greatly, it can be judged that the frequency drift has arisen clearly.

0027 In the clock reproduction circuit concerning this invention, it judged that the clear frequency drift would have occurred, for example on the basis of 0.7 if the value of the bias Be of error distribution is a larger value than 0.7 (F106), and if it is 0.7 or less value, it will be judged that the clear frequency drift is not generated. That is, in the example shown in drawing 3 (a), the value of the bias Be of error distribution is 0.8, and is judged that the clear frequency drift has arisen.

0028 And when it is judged that the clear frequency drift has occurred, the gain in the gain circuit 3 is set as the value according to the absolute value of error total sigmae (F107). That is, according to the size of the absolute value of error total sigmae, selection setting of the one step in the gain which can be set as two or more steps is carried out. In the example shown in drawing 3 (a), since the value of error total sigmae is 44, it is set as the gain of the step according to this value.

0029 On the other hand, when the value of the bias Be of error distribution is 0.7 or less value in F106, jitter width J is calculated after that, and the stable gain Ga over jitter width J and the permissible gain Gb over jitter width J are set up (F108). That is, as shown in drawing 3 (b), in the case of error distribution, since the value of the bias Be of error distribution is 0.2, it is judged that the clear frequency drift is not produced, but a big jitter may be included even when the frequency drift has not arisen. Therefore, it is necessary to set up the gain according to jitter width.

0030 Here, when the gain which can obtain a stable clock to certain jitter width J is searched for experimentally, if jitter width doubles, it turns out that a stable gain serves as half. That is, since the stable gain Ga over jitter width J is in inverse proportion to jitter width J, it becomes as follows.

Ga=a/J (a is a constant)

0031 Since it turns out that it is similarly in inverse proportion to jitter width J when the permissible gain to which a clock is not sharply changed too much to certain jitter width J is searched for experimentally, it becomes as follows.

Gb=b/J (b is a constant)

0032 Although the stable gain Ga and the permissible gain Gb can be set up by defining the above constants a and b by an experiment or an operation beforehand, Since the stable gain Ga is a permissible gain to which, as for the permissible gain Gb, a clock is not sharply changed too much to being a gain which can obtain a stable clock, the relation between the stable gain Ga and the permissible gain Gb becomes as follows.

The thing which is Ga<Gb and for which these values are beforehand held in equipment is also possible.

0033 Next, a step-out is detected by comparing the threshold proportional to jitter width J with the absolute value of error total sigmae. That is, when the absolute value of error total sigmae is over value Jalpha which multiplied jitter width J by the predetermined constant alpha like the graphic display, while judging that it is in a step-out state, in being below value Jalpha which multiplied jitter width J by the predetermined constant alpha, it judges that it is in the state which was able to take the synchronization (F109).

0034 Thus, in the clock reproduction circuit concerning this invention, when jitter width J is a large value, even if the absolute value of error total sigmae is comparatively large, it is judged that it is in the state which was able to take the synchronization. This is for preventing judging it as a step-out under the influence of this big jitter, even if it is in the tendency for the absolute value of error total sigmae to turn into a big value by this big jitter and is a synchronous state, when a big jitter occurs suddenly.

0035 Here, although drawing 3 (c) has taken the synchronization, it shows the state where the big jitter occurred suddenly. Thus, when a big jitter occurs suddenly, the absolute value of error total sigmae turns into a big value under the influence of this jitter, but he judges this state to be a synchronous state, and is trying to avoid unnecessary gain fluctuation in the clock reproduction circuit concerning this invention.

0036 In order to cope with such a big jitter that carries out the heterogenesis, It may be made to judge using

the value of two or more error total not only in error total sigmae in fixed time Ta but this or before by calculating error total over a period longer than fixed time Ta whether it is a synchronous state.

0037 Next, when it is judged that it is in the state which was able to take the synchronization. When the present gain set value is compared with the stable gain Ga over jitter width J (F110) and the present gain set value is over the stable gain Ga, When 1 step lowering (F111) and the present gain set value are below the stable gain Ga about the present gain set value, the present gain is set as the stable gain Ga. Thus, in the state where the synchronization can be taken, a gain is changed in the direction which brings the present gain set value close to the stable gain Ga over jitter width J.

0038 It is 1 step ****** (F114) about the gain set value of the present when the present gain set value is compared with the permissible gain Gb over jitter width J on the other hand when it is distinguished that it is in a step-out state (F113), and the present gain set value is less than the permissible gain Gb.

0039 When the present gain set value is beyond the permissible gain Gb, When the present gain set value is over the permissible gain Gb as compared with the permissible gain Gb (F115), the present gain set value, A gain is not changed when 1 step lowering (F116) and the present gain set value are below the permissible gain Gb about the present gain set value (i.e., when the present gain set value is the same as that of the permissible gain Gb). That is, in a step-out state, a gain is changed in the direction which brings the present gain set value close to the permissible gain Gb over jitter width J.

0040 After performing the above gain control, the maximum Emax of the positive error number Nep, negative error number Nen, total-number-of-error Ne, error total sigmae, and an error and the minimum Emin of an error are initialized (F117), and detection of the new error signal in F102 is resumed.

0041 Thus, in the clock reproduction circuit concerning this invention. Since it judges whether it is a synchronous state in the relation between jitter width J and the absolute value of error total and a gain is changed into the suitable desired value according to jitter width J in each state, Even when the big jitter has occurred in input MPEG 2-TS, the gain in the gain circuit 3 can be set as a suitable value.

0042 And after the value of an error signal is adjusted with the gain set up by doing in this way, it becomes possible to supply the analog signal through digital LPF4 and D/A converter 5 to the voltage controlled oscillator 6, and to obtain quickly the clock which synchronized with the system clock by the side of coding equipment.

0043 When the clear frequency drift had not occurred in F106 in drawing 2 in the above embodiment and it is distinguished, Although the example which performed gain setting according to jitter width was shown, when not only this but the clear frequency drift had not occurred and it is distinguished (i.e., when it is a with a value of 0.7 or less of the bias Be of error distribution value in F106), method control of 1 step ****** may be simply performed for a gain. It becomes possible it to become possible to make a suitable gain set up to the jitter of the grade which is also such control, and to make data processing reduce.

0044 It cannot be overemphasized that it does not matter whether the composition for performing the above gain setting processing is the composition by hardware or is the composition by software. It cannot be overemphasized that the clock reproduction circuit concerning this invention is applicable to image audio equipment, such as D-VHS (registered trademark) provided with the bus interface based on IEEE1394 and a set top box, or other connection devices.

0045

Brief Description of the Drawings

Drawing 1 It is a figure for explaining the composition of the clock reproduction circuit concerning this invention.

Drawing 2 It is a figure for explaining operation of the gain setting circuit 7.

Drawing 3 It is a figure showing distribution of an error signal.

Drawing 4 It is a figure for explaining the composition of the conventional clock reproduction circuit.

Explanations of letters or numerals

1 -- Subtraction machine
2 -- STC counter
3 -- Gain circuit
4 -- Digital LPF
5 -- D/A converter
6 -- Voltage controlled oscillator
7 -- Gain setting circuit

Drawing 1

For drawings please refer to the original document.

Drawing 3

For drawings please refer to the original document.

Drawing 2

For drawings please refer to the original document.

Drawing 4

For drawings please refer to the original document.

For drawings please refer to the original document.
